IN THE CLAIMS

Please amend the claims as follows:

Claims 1-3. (Canceled)

4. (Currently Amended) A computer-implemented method of preparing a circuit model for simulation comprising:

decomposing the circuit model having a number of latches into a plurality of extended latch boundary components; and

partitioning the plurality of extended latch boundary components using a bin-packing heuristic, ~~The method of claim 1,~~ wherein using the [[a]] bin-packing heuristic comprises[[:]]

constructing a plurality of seeds from the plurality of extended latch boundary components[[;]] and

merging the plurality of extended latch boundary components with the plurality of seeds.

5. (Currently Amended) A computer-implemented method of preparing a circuit model for simulation comprising:

decomposing the circuit model having a number of latches into a plurality of extended latch boundary components; and

partitioning the plurality of extended latch boundary components using a bin-packing heuristic, ~~The method of claim 1,~~ wherein decomposing the [[a]] circuit model having a number of latches into a plurality of extend latch boundary components comprises[[:]]

identifying an extended latch boundary component that meets a size constraint for at least one of a plurality of hierarchical cells.

6. (Original) The method of claim 5, wherein partitioning the plurality of extended latch boundary components comprises:

grouping the plurality of extended latch boundary components into a plurality of partitions by approximately equalizing the number of latches in each of the plurality of partitions.

7. (Currently Amended) A computer-implemented method of preparing a circuit model for simulation comprising:

decomposing the circuit model having a number of latches into a plurality of extended latch boundary components; and

partitioning the plurality of extended latch boundary components using a bin-packing heuristic, ~~The method of claim 1,~~ wherein partitioning the plurality of extended latch boundary components comprises[[:]]

grouping the plurality of extended latch boundary components to form a plurality of partitions, each of the plurality of partitions having a size.

8. (Original) The method of claim 7, wherein partitioning the plurality of extended latch boundary components comprises:

partitioning the plurality of extended latch boundary components by approximately equalizing the number of latches in each of the plurality of partitions, approximately equalizing the latches that are activated in each of the plurality of partitions, and approximately equalizing the size of each of the plurality of partitions.

9. (Currently Amended) A computer-implemented method of preparing a circuit model for simulation comprising:

decomposing the circuit model having a number of latches into a plurality of extended latch boundary components; and

partitioning the plurality of extended latch boundary components using a bin-packing heuristic, ~~The method of claim 1,~~ wherein partitioning the plurality of extended latch boundary components comprises[[:]]

partitioning the plurality of extended latch boundary components based on activity load balancing.

Claims 10 -11. (Canceled)

12. (Currently Amended) A computer-implemented method of preparing a circuit model for simulation, the circuit model having a model size, comprising:

merging a plurality of extended latch boundary components into a plurality of partitions having a partition size using a bin-packing heuristic;

maintaining a load balance within the plurality of partitions;

reducing circuit overlap within the plurality of partitions; and ~~The method of claim 11, further comprising:~~

adjusting the load balance to obtain a partition size of less than about 110% of the model size.

13. (Original) The method of claim 12, further comprising:

adjusting the load balance to obtain a partition size of less than about 120% of the model size.

14. (Canceled)

15. (Currently Amended) A computer-implemented method of preparing a circuit model for a simulation having a total simulation time, the method comprising:

grouping a plurality of extended latch boundary components into a plurality of partitions using a bin-packing heuristic;

reducing the communication time within the plurality of partitions by adjusting the grouping; and ~~The method of claim 14, further comprising:~~

reducing the communication time within the plurality of partitions to less than about ten percent of the total simulation time by adjusting the grouping.

Claims 16-18. (Canceled)

19. (Currently Amended) A computer-implemented method of sharing a repeated circuit structure among partitions created using a bin-packing heuristic in a circuit model, the method comprising:

expanding the repeated circuit structure once to form an expanded circuit structure; and

grafting the expanded circuit structure to the circuit model as needed, ~~The method of claim 18,~~ wherein grafting the expanded circuit structure to the circuit model as needed comprises[[:]]

copying a table representing the expanded circuit structure into the circuit model.

20. (Currently Amended) A computer-implemented method of sharing a repeated circuit structure among partitions created using a bin-packing heuristic in a circuit model, the method comprising:

expanding the repeated circuit structure once to form an expanded circuit structure; and

grafting the expanded circuit structure to the circuit model as needed, ~~The method of claim 18,~~ wherein grafting the expanded circuit structure to the circuit model as needed comprises[[:]]

altering a table representing the circuit model to add the expanded circuit structure.

Claims 21-23. (Canceled)

24. (Original) A computer system comprising:

a processor unit;

a dicing unit operably coupled to the processor unit, capable of executing on the processor unit, and capable of decomposing a circuit model into a plurality of extended latch boundary components, and capable of partitioning the plurality of extended latch boundary components; and

a simulation unit operably coupled to the dicing unit and the processor unit, and capable of executing on the processor unit.

25. (Original) The computer system of claim 24, wherein the processor unit is a plurality of distributed processor units.

26. (Original) The computer system of claim 25, wherein the dicing unit is capable of load balancing.

27. (Original) The computer system of claim 26, wherein the dicing unit is capable of activity load balancing.

28. (Canceled)